

## EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	105	((variable near3 capacit\$3) near5 delay) same clock	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/30 10:07
L2	10	1.bsum.	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/30 10:04
S1	0	"10609058"	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/28 12:10
S2	1	"10/609058"	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/28 12:53
S3	352	(symmetric\$5 near3 (clock or tim\$3)) same (convert\$3 or conversion or multiplex\$3 or demultiplex\$3 or de-multiplex\$3)	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/28 13:08
S4	4772	(skew\$3) same (convert\$3 or conversion or multiplex\$3 or demultiplex\$3 or de-multiplex\$3)	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/28 13:09
S5	326	S4 and "370"/\$.ccls.	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/28 13:08
S6	64	((multistage or multi-stage or (multi adj stage)) near3 multiplex\$3).bsum.	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/28 13:21
S7	882	370/537.ccls.	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/28 13:25
S8	5	S7 and ((multistage or multi-stage or (multi adj stage)) near3 multiplex\$3)	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/28 13:25
S9	114	370/540.ccls.	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/28 13:29

## EAST Search History

S10	0	S9 and ((multistage or multi-stage or (multi adj stage)) near3 multiplex\$3)	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/28 13:29
S11	209	370/539.ccls.	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/28 14:15
S12	5	S11 and ((multistage or multi-stage or (multi adj stage)) near3 multiplex\$3)	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/28 13:35
S13	8	S11 and ((multistage or multi-stage or (multi\$3 adj stage)) near3 multiplex\$3)	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/28 13:36
S14	1	S9 and ((multistage or multi-stage or (multi\$3 adj stage)) near3 multiplex\$3)	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/28 13:36
S15	6	S7 and ((multistage or multi-stage or (multi\$3 adj stage)) near3 multiplex\$3)	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/28 13:45
S16	311	((multistage or multi-stage or (multi\$3 adj stage)) near3 multiplex\$3)	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/28 13:39
S17	98	((multistage or multi-stage or (multi\$3 adj stage)) near3 multiplex\$3).bsum.	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/28 13:39
S18	366	370/388.ccls.	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/28 13:45
S19	3	S18 and ((multistage or multi-stage or (multi\$3 adj stage)) near3 multiplex\$3)	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/28 13:46
S20	108	370/535.ccls. and ( (delay\$3 or skew\$3) near3 (clock or timing))	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/28 14:50
S21	526	370/535.ccls. and ( (multiplex\$3 or mux or demultiplex\$3 or de-multiplex\$3 or demux) near2 (plural\$3 or multi\$3) )	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/28 14:55

## EAST Search History

S22	496	370/535.ccls. and ( (multiplex\$3 or mux or demultiplex\$3 or de-multiplex\$3 or demux) near2 (plural\$3 or multi\$3) ) and ( (clock or timing or control or selector) )	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/28 14:57
S23	530	370/535.ccls. and ( (multiplex\$3 or mux or demultiplex\$3 or de-multiplex\$3 or demux or conversion or convert\$3) near2 (plural\$3 or multi\$3) ) and ( (clock or timing or control or selector) )	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/28 14:58
S24	226	370/535.ccls. and ( (multiplex\$3 or mux or demultiplex\$3 or de-multiplex\$3 or demux or conversion or convert\$3) near2 (plural\$3 or multi\$3) ) same ( (clock or timing or control or selector) )	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/28 15:43
S25	100	370/535.ccls. and ( (multiplex\$3 or mux or demultiplex\$3 or de-multiplex\$3 or demux or conversion or convert\$3) near2 (plural\$3 or multi\$3) ) and ( (clock or timing or control or selector) near5 (delay\$3 or skew\$3 or lag\$3) )	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/28 15:53
S26	8	370/535.ccls. and ( (multiplex\$3 or mux or demultiplex\$3 or de-multiplex\$3 or demux or conversion or convert\$3) near2 (plural\$3 or multi\$3) ) same ( (clock or timing or control or selector) near5 (delay\$3 or skew\$3 or lag\$3) )	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/28 16:04
S27	10	370/537.ccls. and ( (multiplex\$3 or mux or demultiplex\$3 or de-multiplex\$3 or demux or conversion or convert\$3) near2 (plural\$3 or multi\$3) ) same ( (clock or timing or control or selector) near5 (delay\$3 or skew\$3 or lag\$3) )	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/28 16:44
S28	4	370/539.ccls. and ( (multiplex\$3 or mux or demultiplex\$3 or de-multiplex\$3 or demux or conversion or convert\$3) near2 (plural\$3 or multi\$3) ) same ( (clock or timing or control or selector) near5 (delay\$3 or skew\$3 or lag\$3) )	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/28 16:46

## EAST Search History

S29	2	370/540.ccls. and ( (multiplex\$3 or mux or demultiplex\$3 or de-multiplex\$3 or demux or conversion or convert\$3) near2 (plural\$3 or multi\$3) ) same ( (clock or timing or control or selector) near5 (delay\$3 or skew\$3 or lag\$3) )	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/28 16:49
S30	2	370/541.ccls. and ( (multiplex\$3 or mux or demultiplex\$3 or de-multiplex\$3 or demux or conversion or convert\$3) near2 (plural\$3 or multi\$3) ) same ( (clock or timing or control or selector) near5 (delay\$3 or skew\$3 or lag\$3) )	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/28 16:49
S31	7	370/541.ccls. and ( (multiplex\$3 or mux or demultiplex\$3 or de-multiplex\$3 or demux or conversion or convert\$3) ) same ( (clock or timing or control or selector) near5 (delay\$3 or skew\$3 or lag\$3) )	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/28 16:52
S32	16	370/539.ccls. and ( (multiplex\$3 or mux or demultiplex\$3 or de-multiplex\$3 or demux or conversion or convert\$3) ) same ( (clock or timing or control or selector) near5 (delay\$3 or skew\$3 or lag\$3) )	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/28 16:55
S33	72	370/537.ccls. and ( (multiplex\$3 or mux or demultiplex\$3 or de-multiplex\$3 or demux or conversion or convert\$3) ) same ( (clock or timing or control or selector) near5 (delay\$3 or skew\$3 or lag\$3) )	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/29 10:28
S34	98	370/517.ccls. and ( (multiplex\$3 or mux or demultiplex\$3 or de-multiplex\$3 or demux or conversion or convert\$3) ) same ( (clock or timing or control or selector) near5 (delay\$3 or skew\$3 or lag\$3) )	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/29 14:31

## EAST Search History

S35	4	370/517.ccls. and ( (multiplex\$3 or mux or demultiplex\$3 or de-multiplex\$3 or demux or conversion or convert\$3) ) and ( (clock or timing or control or selector) near5 (delay\$3 or skew\$3 or lag\$3) ) same capacitor)	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/29 12:54
S36	2	370/518.ccls. and ( (multiplex\$3 or mux or demultiplex\$3 or de-multiplex\$3 or demux or conversion or convert\$3) ) and ( (clock or timing or control or selector) near5 (delay\$3 or skew\$3 or lag\$3) ) same capacitor)	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/29 12:55
S37	2	370/519.ccls. and ( (multiplex\$3 or mux or demultiplex\$3 or de-multiplex\$3 or demux or conversion or convert\$3) ) and ( (clock or timing or control or selector) near5 (delay\$3 or skew\$3 or lag\$3) ) same capacitor)	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/29 12:57
S38	4339	( (multiplex\$3 or mux or demultiplex\$3 or de-multiplex\$3 or demux or conversion or convert\$3) ) and ( (clock or timing or control or selector) near5 (delay\$3 or skew\$3 or lag\$3) ) same capacitor)	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/29 12:57
S39	62	"370"/\$.ccls. and ( (multiplex\$3 or mux or demultiplex\$3 or de-multiplex\$3 or demux or conversion or convert\$3) ) and ( (clock or timing or control or selector) near5 (delay\$3 or skew\$3 or lag\$3) ) same capacitor)	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/29 13:00
S40	272	"375"/\$.ccls. and ( (multiplex\$3 or mux or demultiplex\$3 or de-multiplex\$3 or demux or conversion or convert\$3) ) and ( (clock or timing or control or selector) near5 (delay\$3 or skew\$3 or lag\$3) ) same capacitor)	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/29 12:57

## EAST Search History

S41	13	"370"/\$.ccls. and ( (multiplex\$3 or mux or demultiplex\$3 or de-multiplex\$3 or demux or conversion or convert\$3) ) and ( (clock or timing or control or selector) near5 (delay\$3 or skew\$3 or lag\$3) ) near5 capacitor)	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/29 13:06
S42	1048	( (multiplex\$3 or mux or demultiplex\$3 or de-multiplex\$3 or demux or conversion or convert\$3) ) and ( (clock or timing or control or selector) near5 (delay\$3 or skew\$3 or lag\$3) ) near5 capacitor)	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/29 13:00
S43	53	"375"/\$.ccls. and ( (multiplex\$3 or mux or demultiplex\$3 or de-multiplex\$3 or demux or conversion or convert\$3) ) and ( (clock or timing or control or selector) near5 (delay\$3 or skew\$3 or lag\$3) ) near5 capacitor)	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/29 13:06
S44	340	370/517.ccls. and (multiplex\$3 or mux or demultiplex\$3 or de-multiplex\$3 or demux or conversion or convert\$3)	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/29 13:31
S45	276	370/517.ccls. and (multiplex\$3 or mux or demultiplex\$3 or de-multiplex\$3 or demux)	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/29 13:34
S46	75	370/517.ccls. and ( (multiple or plural\$5) near3 (multiplex\$3 or mux or demultiplex\$3 or de-multiplex\$3 or demux) )	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/29 14:02
S47	33	370/518.ccls. and ( (multiple or plural\$5) near3 (multiplex\$3 or mux or demultiplex\$3 or de-multiplex\$3 or demux) )	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/29 14:11
S48	30	370/519.ccls. and ( (multiple or plural\$5) near3 (multiplex\$3 or mux or demultiplex\$3 or de-multiplex\$3 or demux) )	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/29 14:11
S49	23349	( (multiplex\$3 or mux or demultiplex\$3 or de-multiplex\$3 or demux or conversion or convert\$3) ) same ( (clock or timing or control or selector) near5 (delay\$3 or skew\$3 or lag\$3) )	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/29 14:31

## EAST Search History

S50	125	( (multiplex\$3 or mux or demultiplex\$3 or de-multiplex\$3 or demux or conversion or convert\$3) ) same ( (clock or timing or control or selector) near5 (delay\$3 or skew\$3 or lag\$3) near5 capacitor)	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/29 14:42
S51	0	370/541.ccls. and ( (multiplex\$3 or mux or demultiplex\$3 or de-multiplex\$3 or demux or conversion or convert\$3) ) same ( (clock or timing or control or selector) near5 (delay\$3 or skew\$3 or lag\$3) near5 capacitor)	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/29 14:42
S52	7	370/541.ccls. and ( (multiplex\$3 or mux or demultiplex\$3 or de-multiplex\$3 or demux or conversion or convert\$3) ) same ( (clock or timing or control or selector) near5 (delay\$3 or skew\$3 or lag\$3))	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/29 16:19
S53	1	10/612156	US-PGPUB; USPAT; JPO; IBM_TDB	OR	ON	2007/03/29 16:27

Day : Friday  
Date: 3/30/2007

# **PALM INTRANET**

Time: 13:07:30

## Inventor Name Search Result

Your Search was:

Last Name = YIN

First Name = GUANGMING

Application#	Patent#	Status	Date Filed	Title	Inventor Name
<u>08536405</u>	<u>5614864</u>	150	09/29/1995	SINGLE-ENDED TO DIFFERENTIAL CONVERTER WITH RELAXED COMMON-MODE INPUT REQUIREMENTS	YIN, GUANGMING
<u>09410136</u>	<u>6690949</u>	150	09/30/1999	SYSTEM AND PROCESS FOR SUPPORTING MULTIPLE WIRELESS STANDARDS WITH A SINGLE CIRCUIT ARCHITECTURE	YIN, GUANGMING
<u>09785690</u>	<u>6437720</u>	150	02/16/2001	CODE INDEPENDENT CHARGE TRANSFER SCHEME FOR SWITCHED-CAPACITOR DIGITAL-TO-ANALOG CONVERTER	YIN, GUANGMING
<u>09814196</u>	<u>6754287</u>	150	03/21/2001	METHOD AND APPARATUS FOR PRODUCING A MODULATED SIGNAL	YIN, GUANGMING
<u>09814921</u>	<u>6535735</u>	150	03/22/2001	CRITICAL PATH ADAPTIVE POWER CONTROL	YIN, GUANGMING
<u>09881932</u>	<u>6651021</u>	150	06/15/2001	SYSTEM USING ADAPTIVE CIRCUITRY TO IMPROVE PERFORMANCE AND PROVIDE LINEARITY AND DYNAMIC RANGE ON DEMAND	YIN, GUANGMING
<u>10028806</u>	<u>6624699</u>	150	10/25/2001	CURRENT-CONTROLLED CMOS WIDEBAND DATA AMPLIFIER CIRCUITS	YIN, GUANGMING
<u>10177031</u>	<u>6911855</u>	150	06/21/2002	CURRENT-CONTROLLED CMOS CIRCUIT USING HIGHER VOLTAGE SUPPLY IN LOW VOLTAGE CMOS PROCESS	YIN, GUANGMING



<u>10229257</u>	<u>6897697</u>	150	08/26/2002	CURRENT -CONTROLLED CMOS CIRCUIT USING HIGHER VOLTAGE SUPPLY IN LOW VOLTAGE CMOS PROCESS	YIN, GUANGMING
<u>10243086</u>	<u>6870415</u>	150	09/12/2002	Delay generator with controlled delay circuit	YIN, GUANGMING
<u>10361255</u>	Not Issued	41	02/10/2003	High-speed serial bit stream multiplexing and demultiplexing integrated circuits	YIN, GUANGMING
<u>10361463</u>	Not Issued	41	02/10/2003	Source centered clock supporting quad 10 GBPS serial interface	YIN, GUANGMING
<u>10445771</u>	Not Issued	30	05/27/2003	Signal delay structure in high speed bit stream demultiplexer	YIN, GUANGMING
<u>10448640</u>	<u>6943587</u>	150	05/30/2003	SWITCHABLE POWER DOMAINS FOR 1.2V AND 3.3V PAD VOLTAGES	YIN, GUANGMING
<u>10456803</u>	Not Issued	60	06/06/2003	Method and system for pattern-independent phase adjustment in a clock and data recovery (CDR) circuit	YIN, GUANGMING
<u>10456804</u>	<u>6930512</u>	150	06/06/2003	ONE-LEVEL ZERO-CURRENT-STATE EXCLUSIVE OR (XOR) GATE	YIN, GUANGMING
<u>10609058</u>	Not Issued	30	06/28/2003	Symmetrical clock distribution in multi-stage high speed data conversion circuits	YIN, GUANGMING
<u>10618462</u>	<u>7109799</u>	150	07/11/2003	CURRENT-CONTROLLED CMOS WIDEBAND DATA AMPLIFIER CIRCUITS	YIN, GUANGMING
<u>10623992</u>	Not Issued	41	07/21/2003	Voltage controlled oscillator for use in phase locked loop	YIN, GUANGMING
<u>10639079</u>	<u>6909332</u>	150	08/12/2003	SYSTEM AND METHOD FOR TUNING OUTPUT DRIVERS USING VOLTAGE CONTROLLED OSCILLATOR CAPACITOR SETTINGS	YIN, GUANGMING
<u>10778419</u>	Not Issued	30	02/13/2004	System and method for testing the operation of a DLL-based interface	YIN, GUANGMING
<u>10841766</u>	<u>7034606</u>	150	05/07/2004	NOVEL VGA-CTF COMBINATION CELL FOR 10 GB/S SERIAL DATA RECEIVERS	YIN, GUANGMING

<u>10852275</u>	<u>6980053</u>	150	05/24/2004	ADAPTABLE VOLTAGE CONTROL FOR A VARIABLE GAIN AMPLIFIER	YIN, GUANGMING
<u>10876790</u>	<u>6982583</u>	150	06/25/2004	CURRENT-CONTROLLED CMOS CIRCUIT USING HIGHER VOLTAGE SUPPLY IN LOW VOLTAGE CMOS PROCESS	YIN, GUANGMING
<u>10880959</u>	Not Issued	30	06/30/2004	High speed receive equalizer architecture	YIN, GUANGMING
<u>11057968</u>	<u>6989715</u>	150	02/15/2005	ONE-LEVEL ZERO-CURRENT-STATE EXCLUSIVE OR (XOR) GATE	YIN, GUANGMING
<u>11078151</u>	<u>7098692</u>	150	03/11/2005	SWITCHABLE POWER DOMAINS FOR 1.2V AND 3.3V PAD VOLTAGES	YIN, GUANGMING
<u>11084369</u>	Not Issued	61	03/18/2005	Delay generator with symmetric signal paths	YIN, GUANGMING
<u>11120738</u>	Not Issued	30	05/03/2005	System and method for tuning output drivers using voltage controlled oscillator capacitor settings	YIN, GUANGMING
<u>11133723</u>	<u>7142013</u>	150	05/20/2005	ONE-LEVEL ZERO-CURRENT-STATE EXCLUSIVE OR (XOR) GATE	YIN, GUANGMING
<u>11239927</u>	<u>7135926</u>	150	09/29/2005	ADAPTABLE VOLTAGE CONTROL FOR A VARIABLE GAIN AMPLIFIER	YIN, GUANGMING
<u>11559195</u>	Not Issued	30	11/13/2006	ADAPTABLE VOLTAGE CONTROL FOR A VARIABLE GAIN AMPLIFIER	YIN, GUANGMING
<u>60247098</u>	Not Issued	159	11/10/2000	Transmit level control of a data carrier for power-line networking	YIN, GUANGMING
<u>60401732</u>	Not Issued	159	08/06/2002	High-speed serial bit stream multiplexing and demultiplexing integrated circuits	YIN, GUANGMING
<u>60401735</u>	Not Issued	159	08/06/2002	Source centered clock supporting quad 10 GBPS serial interface	YIN, GUANGMING
<u>60403455</u>	Not Issued	159	08/12/2002	Switchable power domains for 1.2V and 3.3V pad voltages	YIN, GUANGMING
<u>60403457</u>	Not	159	08/12/2002	Signal delay structure in high	YIN, GUANGMING

	Issued			speed bit stream demultiplexer with hybrid high-speed/low-speed output latch	
<a href="#">60424562</a>	Not Issued	159	11/06/2002	Method and apparatus for a one-level tri-state exclusive or (XOR) gate	YIN, GUANGMING
<a href="#">60424563</a>	Not Issued	159	11/06/2002	Method and system for pattern-independent phase adjustment in a clock and data recovery (CDR) circuit	YIN, GUANGMING
<a href="#">60576176</a>	Not Issued	159	06/02/2004	High speed receive equalizer architecture	YIN, GUANGMING

Inventor Search Completed: No Records to Display.

<b>Search Another: Inventor</b>	<b>Last Name</b>	<b>First Name</b>	<input type="button" value="Search"/>
	<input type="text" value="YIN"/>	<input type="text" value="GUANGMING"/>	

To go back use Back button on your browser toolbar.

Back to [PALM](#) | [ASSIGNMENT](#) | [OASIS](#) | [Home page](#)

Day : Friday  
Date: 3/30/2007


**PALM INTRANET**

Time: 13:07:39

**Inventor Name Search Result**

Your Search was:

Last Name = ZHANG

First Name = BO

Application#	Patent#	Status	Date Filed	Title	Inventor Name
<a href="#">07469157</a>	Not Issued	161	01/24/1990	WINDOW BLIND WITH DECORATIVE PICTURE ON BLIND LEAVES	ZHANG, BO
<a href="#">08985724</a>	Not Issued	161	12/05/1997	HI-LO TRANSMISSION	ZHANG, BO
<a href="#">09081542</a>	<a href="#">6181218</a>	150	05/19/1998	HIGH-LINEARITY, LOW-SPREAD VARIABLE CAPACITANCE ARRAY	ZHANG, BO
<a href="#">09315006</a>	<a href="#">6414822</a>	150	05/19/1999	MAGNETIC MICROACTUATOR	ZHANG, BO
<a href="#">09406954</a>	<a href="#">6452424</a>	150	09/28/1999	METHOD AND APPARATUS FOR MULTIPLE CHANNEL SIGNAL PROCESSING	ZHANG, BO
<a href="#">09572860</a>	<a href="#">6721357</a>	150	05/18/2000	CONSTELLATION GENERATION AND RE-EVALUATION	ZHANG, BO
<a href="#">09579529</a>	<a href="#">6721363</a>	150	05/26/2000	RECEIVER CODEC SUPER SET CONSTELLATION GENERATOR	ZHANG, BO
<a href="#">09615627</a>	<a href="#">6526109</a>	150	12/05/2000	METHOD AND APPARATUS FOR HYBRID SMART CENTER LOOP FOR CLOCK DATA RECOVERY	ZHANG, BO
<a href="#">09615631</a>	<a href="#">6316966</a>	150	07/13/2000	Apparatus and method for servo-controlled self-centering phase detector	ZHANG, BO
<a href="#">09721313</a>	Not Issued	161	11/22/2000	High-linearity, low-spread variable capacitance array	ZHANG, BO
<a href="#">09785690</a>	<a href="#">6437720</a>	150	02/16/2001	CODE INDEPENDENT CHARGE TRANSFER SCHEME FOR SWITCHED-CAPACITOR DIGITAL-TO-ANALOG CONVERTER	ZHANG, BO

<u>09910436</u>	<u>6614371</u>	150	07/19/2001	SYNCHRONOUS DATA SERIALIZATION CIRCUIT	ZHANG, BO
<u>10099348</u>	Not Issued	71	03/14/2002	Dialog manager for interactive dialog with computer user	ZHANG, BO
<u>10099673</u>	<u>7019749</u>	150	03/14/2002	CONVERSATIONAL INTERFACE AGENT	ZHANG, BO
<u>10243086</u>	<u>6870415</u>	150	09/12/2002	Delay generator with controlled delay circuit	ZHANG, BO
<u>10243281</u>	<u>6781420</u>	150	09/12/2002	SYMMETRIC DIFFERENTIAL LOGIC CIRCUITS	ZHANG, BO
<u>10243495</u>	Not Issued	61	09/13/2002	Phase interpolater and applications thereof	ZHANG, BO
<u>10373229</u>	Not Issued	41	02/24/2003	Method and system to efficiently modulate data while reducing DC drift	ZHANG, BO
<u>10390490</u>	Not Issued	41	03/17/2003	Loop back testing structure for high-speed serial bit stream TX and RX chip set	ZHANG, BO
<u>10431103</u>	<u>6867716</u>	150	05/06/2003	SYNCHRONOUS DATA SERIALIZATION CIRCUIT	ZHANG, BO
<u>10448755</u>	<u>6958303</u>	150	05/30/2003	ELECTRO-STATIC DISSIPATIVE CERAMIC PRODUCTS AND METHODS	ZHANG, BO
<u>10609058</u>	Not Issued	30	06/28/2003	Symmetrical clock distribution in multi-stage high speed data conversion circuits	ZHANG, BO
<u>10611120</u>	Not Issued	41	06/30/2003	Flexibly resizeable vector graphics	ZHANG, BO
<u>10639079</u>	<u>6909332</u>	150	08/12/2003	SYSTEM AND METHOD FOR TUNING OUTPUT DRIVERS USING VOLTAGE CONTROLLED OSCILLATOR CAPACITOR SETTINGS	ZHANG, BO
<u>10778419</u>	Not Issued	30	02/13/2004	System and method for testing the operation of a DLL-based interface	ZHANG, BO
<u>10804914</u>	Not Issued	30	03/19/2004	Receiver codec super set constellation generator	ZHANG, BO
<u>10882428</u>	<u>7038510</u>	150	07/02/2004	PHASE ADJUSTMENT METHOD AND CIRCUIT FOR DLL-BASED SERIAL DATA LINK TRANSCEIVERS	ZHANG, BO
<u>10882926</u>	Not Issued	30	06/30/2004	Dynamic player groups for interest management in multi-character virtual environments	ZHANG, BO

<u>10884432</u>	<u>7138834</u>	150	07/02/2004	SYMMETRIC DIFFERENTIAL LOGIC CIRCUITS	ZHANG, BO
<u>10918840</u>	Not Issued	30	08/13/2004	Perceptually based approach for planar shape morphing	ZHANG, BO
<u>10919093</u>	Not Issued	80	08/16/2004	Synchronous data serialization circuit	ZHANG, BO
<u>10981128</u>	<u>7026339</u>	150	11/03/2004	INHIBITORS OF HCV NS5B POLYMERASE	ZHANG, BO
<u>11016279</u>	Not Issued	30	12/17/2004	Air humidifying system for fuel cell stack	ZHANG, BO
<u>11019761</u>	Not Issued	160	12/22/2004	Power line communications device in which physical communications protocol layer operation is dynamically selectable	ZHANG, BO
<u>11084369</u>	Not Issued	61	03/18/2005	Delay generator with symmetric signal paths	ZHANG, BO
<u>11096467</u>	Not Issued	30	04/01/2005	Method and system for rate control in a video encoder	ZHANG, BO
<u>11096468</u>	Not Issued	30	04/01/2005	Method and system for frame/field coding	ZHANG, BO
<u>11096476</u>	Not Issued	30	04/01/2005	Method and system for motion estimation in a video encoder	ZHANG, BO
<u>11096603</u>	Not Issued	30	04/01/2005	Method and system for formatting encoded video data	ZHANG, BO
<u>11096825</u>	Not Issued	30	04/01/2005	Method and system for motion estimation in a video encoder	ZHANG, BO
<u>11113733</u>	Not Issued	30	04/25/2005	Method and system for encoding video data	ZHANG, BO
<u>11120738</u>	Not Issued	30	05/03/2005	System and method for tuning output drivers using voltage controlled oscillator capacitor settings	ZHANG, BO
<u>11127759</u>	Not Issued	30	05/11/2005	Method for forwarding multimedia messages between different multimedia messaging service centers	ZHANG, BO
<u>11127760</u>	Not Issued	30	05/11/2005	Method for forwarding multimedia messages between multimedia messaging service centers	ZHANG, BO
<u>11195521</u>	Not Issued	41	08/02/2005	Synthesis of polyhydroxyalkanoates in the cytosol of yeast	ZHANG, BO
<u>11196893</u>	Not Issued	41	08/04/2005	Conversational interface agent	ZHANG, BO

<a href="#">11230950</a>	Not Issued	120	09/19/2005	Electro-static dissipative ceramic products and methods	ZHANG, BO
<a href="#">11241142</a>	Not Issued	30	09/30/2005	On-chip capacitor structure	ZHANG, BO
<a href="#">11401959</a>	Not Issued	41	04/12/2006	Phase adjustment method and circuit for DLL-based serial data link transceivers	ZHANG, BO
<a href="#">11411648</a>	Not Issued	20	04/26/2006	On-chip capacitor structure with adjustable capacitance	ZHANG, BO

[Search and Display More Records.](#)

<b>Search Another: Inventor</b>	<b>Last Name</b>	<b>First Name</b>	<input type="button" value="Search"/>
	<input type="text" value="ZHANG"/>	<input type="text" value="BO"/>	

To go back use Back button on your browser toolbar.

Back to [PALM](#) | [ASSIGNMENT](#) | [OASIS](#) | [Home page](#)

Day : Friday  
Date: 3/30/2007


**PALM INTRANET**

Time: 13:07:49

**Inventor Name Search Result**

Your Search was:

Last Name = NEJAD

First Name = MOHAMMAD

Application#	Patent#	Status	Date Filed	Title	Inventor Name
<a href="#">10349450</a>	Not Issued	41	01/22/2003	Signal line selection and polarity change of natural bit ordering in high-speed serial bit stream multiplexing and demultiplexing integrated circuits	NEJAD, MOHAMMAD
<a href="#">10361255</a>	Not Issued	41	02/10/2003	High-speed serial bit stream multiplexing and demultiplexing integrated circuits	NEJAD, MOHAMMAD
<a href="#">10361463</a>	Not Issued	41	02/10/2003	Source centered clock supporting quad 10 GBPS serial interface	NEJAD, MOHAMMAD
<a href="#">10448640</a>	<a href="#">6943587</a>	150	05/30/2003	SWITCHABLE POWER DOMAINS FOR 1.2V AND 3.3V PAD VOLTAGES	NEJAD, MOHAMMAD
<a href="#">10602227</a>	Not Issued	41	06/24/2003	Multi-stage multiplexing chip set having switchable forward/reverse clock relationship	NEJAD, MOHAMMAD
<a href="#">10609058</a>	Not Issued	30	06/28/2003	Symmetrical clock distribution in multi-stage high speed data conversion circuits	NEJAD, MOHAMMAD
<a href="#">11078151</a>	<a href="#">7098692</a>	150	03/11/2005	SWITCHABLE POWER DOMAINS FOR 1.2V AND 3.3V PAD VOLTAGES	NEJAD, MOHAMMAD
<a href="#">60401732</a>	Not Issued	159	08/06/2002	High-speed serial bit stream multiplexing and demultiplexing integrated circuits	NEJAD, MOHAMMAD
<a href="#">60401735</a>	Not Issued	159	08/06/2002	Source centered clock supporting quad 10 GBPS serial interface	NEJAD, MOHAMMAD
<a href="#">08924028</a>	<a href="#">5950115</a>	150	08/29/1997	GHZ TRANSCEIVER PHASE LOCK LOOP HAVING AUTOFREQUENCY LOCK CORRECTION	NEJAD, MOHAMMAD S.
<a href="#">10353438</a>	Not	41	01/29/2003	Eye monitoring and	NEJAD,



	Issued			reconstruction using CDR and sub-sampling ADC	MOHAMMAD SARHANG
<a href="#">60416931</a>	Not Issued	159	10/08/2002	Eye monitoring and reconstruction using CDR and sub-sampling ADC	NEJAD, MOHAMMAD SARHANG

**Inventor Search Completed: No Records to Display.**


**Search Another: Inventor**

Last Name	First Name	
<input type="text" value="NEJAD"/>	<input type="text" value="MOHAMMAD"/>	<input type="button" value="Search"/>

To go back use Back button on your browser toolbar.

Back to [PALM](#) | [ASSIGNMENT](#) | [OASIS](#) | [Home page](#)

Day : Friday  
Date: 3/30/2007


**PALM INTRANET**

Time: 13:07:59

**Inventor Name Search Result**

Your Search was:

Last Name = CAO

First Name = JUN

Application#	Patent#	Status	Date Filed	Title	Inventor Name
<a href="#">09241658</a>	<a href="#">6700899</a>	150	02/02/1999	BIT SLICE ARBITER	CAO, JUN
<a href="#">09249837</a>	<a href="#">6363077</a>	150	02/12/1999	LOAD BALANCING IN LINK AGGREGATION AND TRUNKING	CAO, JUN
<a href="#">09450527</a>	<a href="#">6246256</a>	150	11/29/1999	QUANTIZED QUEUE LENGTH ARBITER	CAO, JUN
<a href="#">09632665</a>	<a href="#">6760394</a>	150	08/07/2000	CMOS LOCK DETECT WITH DOUBLE PROTECTION	CAO, JUN
<a href="#">09632666</a>	<a href="#">6725408</a>	150	08/07/2000	BUILT-IN SELF-TEST FOR MULTI-CHANNEL TRANCEIVERS WITHOUT DATA ALIGNMENT	CAO, JUN
<a href="#">09772781</a>	<a href="#">6396894</a>	150	01/29/2001	OVERFLOW DETECTOR FOR FIFO	CAO, JUN
<a href="#">09784419</a>	<a href="#">6909852</a>	150	02/15/2001	LINEAR FULL-RATE PHASE DETECTOR AND CLOCK AND DATA RECOVERY CIRCUIT	CAO, JUN
<a href="#">09794948</a>	<a href="#">7009973</a>	150	02/28/2001	SWITCH USING A SEGMENTED RING	CAO, JUN
<a href="#">09826160</a>	<a href="#">6420901</a>	150	04/05/2001	QUANTIZED QUEUE LENGTH ARBITER	CAO, JUN
<a href="#">09861745</a>	<a href="#">6826561</a>	150	05/22/2001	METHOD AND APPARATUS FOR PERFORMING A BINARY SEARCH ON AN EXPANDED TREE	CAO, JUN
<a href="#">09919636</a>	<a href="#">6721380</a>	150	07/31/2001	FULLY DIFFERENTIAL CMOS PHASE-LOCKED LOOP	CAO, JUN
<a href="#">09955693</a>	<a href="#">7092474</a>	150	09/18/2001	LINEAR PHASE DETECTOR FOR HIGH-SPEED CLOCK AND DATA RECOVERY	CAO, JUN
<a href="#">09956374</a>	<a href="#">6696854</a>	150	09/17/2001	METHODS AND CIRCUITRY	CAO, JUN

				FOR IMPLEMENTING FIRST-IN FIRST-OUT STRUCTURE	
<u>09978347</u>	<u>6542043</u>	150	10/16/2001	ALL PMOS FULLY DIFFERENTIAL VOLTAGE CONTROLLED OSCILLATOR	CAO, JUN
<u>10028806</u>	<u>6624699</u>	150	10/25/2001	CURRENT-CONTROLLED CMOS WIDEBAND DATA AMPLIFIER CIRCUITS	CAO, JUN
<u>10041665</u>	<u>6614758</u>	150	01/10/2002	LOAD BALANCING IN LINK AGGREGATION AND TRUNKING	CAO, JUN
<u>10104870</u>	<u>6519311</u>	150	03/21/2002	OVERFLOW DETECTOR FOR FIFO	CAO, JUN
<u>10158845</u>	<u>6570403</u>	150	06/03/2002	QUANTIZED QUEUE LENGTH ARBITER	CAO, JUN
<u>10286597</u>	<u>7154983</u>	150	11/01/2002	METHOD OF OPERATING A FIRST-IN FIRST-OUT (FIFO) CIRCUIT	CAO, JUN
<u>10293163</u>	Not Issued	41	11/12/2002	Phase detector for extended linear response and high-speed data regeneration	CAO, JUN
<u>10293624</u>	Not Issued	71	11/12/2002	Phase detector with delay elements for improved data regeneration	CAO, JUN
<u>10328119</u>	Not Issued	41	12/23/2002	System and method for adjusting phase offsets	CAO, JUN
<u>10445771</u>	Not Issued	30	05/27/2003	Signal delay structure in high speed bit stream demultiplexer	CAO, JUN
<u>10445773</u>	Not Issued	41	05/27/2003	Hybrid high-speed/low-speed output latch in 10 GBPS interface with half rate clock	CAO, JUN
<u>10609058</u>	Not Issued	30	06/28/2003	Symmetrical clock distribution in multi-stage high speed data conversion circuits	CAO, JUN
<u>10618462</u>	<u>7109799</u>	150	07/11/2003	CURRENT-CONTROLLED CMOS WIDEBAND DATA AMPLIFIER CIRCUITS	CAO, JUN
<u>10635465</u>	Not Issued	93	08/07/2003	LOAD BALANCING IN LINK AGGREGATION AND TRUNKING	CAO, JUN
<u>10749965</u>	<u>6963220</u>	150	12/31/2003	METHODS AND CIRCUITRY FOR IMPLEMENTING FIRST-IN FIRST-OUT STRUCTURE	CAO, JUN
<u>10750098</u>	<u>6940306</u>	150	12/31/2003	METHODS AND CIRCUITRY FOR IMPLEMENTING FIRST-	CAO, JUN

				IN FIRST-OUT STRUCTURE	
<u>10759454</u>	Not Issued	30	01/20/2004	Bit slice arbiter	CAO, JUN
<u>10764093</u>	<u>7017098</u>	150	01/23/2004	BUILT-IN SELF-TEST FOR MULTI-CHANNEL TRANSCEIVERS WITHOUT DATA ALIGNMENT	CAO, JUN
<u>10797770</u>	Not Issued	30	03/10/2004	Fully differential CMOS phase-locked loop	CAO, JUN
<u>10843181</u>	<u>6909762</u>	150	05/11/2004	Phase-locked loop circuit	CAO, JUN
<u>10852280</u>	Not Issued	71	05/24/2004	Finite impulse response de-emphasis with inductive shunt peaking for near-end and far-end signal integrity	CAO, JUN
<u>10930980</u>	<u>7190906</u>	150	08/31/2004	LINEAR FULL-RATE PHASE DETECTOR AND CLOCK AND DATA RECOVERY CIRCUIT	CAO, JUN
<u>10937321</u>	Not Issued	41	09/10/2004	Method and apparatus for performing a binary search on an expanded tree	CAO, JUN
<u>10965074</u>	<u>7072885</u>	150	10/15/2004	METHOD AND APPARATUS FOR PERFORMING A BINARY SEARCH ON AN EXPANDED TREE	CAO, JUN
<u>11027193</u>	<u>6963221</u>	150	12/30/2004	METHODS AND CIRCUITRY FOR IMPLEMENTING FIRST-IN FIRST-OUT STRUCTURE	CAO, JUN
<u>11027848</u>	<u>7205792</u>	150	12/31/2004	METHODS AND CIRCUITRY FOR IMPLEMENTING FIRST-IN FIRST-OUT STRUCTURE	CAO, JUN
<u>11027864</u>	<u>7167024</u>	150	12/31/2004	METHODS AND CIRCUITRY FOR IMPLEMENTING FIRST-IN FIRST-OUT STRUCTURE	CAO, JUN
<u>11078483</u>	Not Issued	30	03/14/2005	Pre-learning of values with later activation in a network device	CAO, JUN
<u>11078484</u>	Not Issued	30	03/14/2005	Timestamp metering and rollover protection in a network device	CAO, JUN
<u>11078508</u>	Not Issued	30	03/14/2005	Bookkeeping memory use in a search engine of a network device	CAO, JUN
<u>11081057</u>	Not Issued	30	03/16/2005	Programmable metering behavior based on table lookup	CAO, JUN
<u>11081644</u>	Not Issued	30	03/17/2005	Powerful and expandable pipeline architecture for a network device	CAO, JUN

<a href="#">11082357</a>	<a href="#">7183540</a>	150	03/17/2005	APPARATUS FOR MEASURING PHOTO DIODES' TEMPERATURE DEPENDENCE	CAO, JUN
<a href="#">11084482</a>	Not Issued	30	03/21/2005	Dynamic table sharing of memory space within a network device	CAO, JUN
<a href="#">11117768</a>	<a href="#">7103130</a>	150	04/28/2005	PHASE-LOCKED LOOP CIRCUIT	CAO, JUN
<a href="#">11320398</a>	Not Issued	30	12/28/2005	Current-controlled CMOS (C3MOS) fully differential integrated wideband amplifier/equalizer with adjustable gain and frequency response without additional power or loading	CAO, JUN
<a href="#">11320401</a>	Not Issued	41	12/28/2005	Current-controlled CMOS (C3MOS) fully differential integrated delay cell with variable delay and high bandwidth	CAO, JUN

[Search and Display More Records.](#)

<b>Search Another: Inventor</b>	<b>Last Name</b>	<b>First Name</b>	<input type="button" value="Search"/>
	<input type="text" value="CAO"/>	<input type="text" value="JUN"/>	

To go back use Back button on your browser toolbar.

Back to [PALM](#) | [ASSIGNMENT](#) | [OASIS](#) | [Home page](#)